

PATENT APPLICATION
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Applicant: Jin-Hyuk LEE, Gu-Sung KIM, Dong-Ho LEE and Dong-Hyeon JANG
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Title: METHOD FOR MANUFACTURING A WAFER LEVEL CHIP SCALE PACKAGE

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U.S. PATENT DOCUMENTS

<u>Exam Init</u>	<u>Ref</u>	<u>Document Number</u>	<u>Issue Date</u>	<u>Name</u>	<u>Class</u>	<u>Sub Class</u>
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FOREIGN PATENT DOCUMENTS

<u>Exam Init</u>	<u>Ref</u>	<u>Document Number</u>	<u>Publication Date</u>	<u>Country</u>	<u>Name</u>
—	—	2001-04529	1/15/2001	Korea	Sun-Jin Cho
—	—	2000-65487	11/15/2000	Korea	Lee and Sim
—	—	2000-286283	10/13/2000	Japan	Kuniyasu

OTHER DOCUMENTS

<u>Exam Init</u>	<u>Ref</u>	<u>Author, Title, Date, Pertinent Pages, Etc.)</u>
—	—	English language of Korean Abstract for Korean Patent Publication No. 2001-04529, filed 1/15/2001.
—	—	English language of Korean Abstract for Korean Patent Publication No. 2000-65487, filed 11/15/2000.
—	—	English language of Japanese Abstract for Japanese Patent Publication No. 2000-286283, filed 10/13/2000.

Examiner: _____

Date Considered: _____